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09/144,579	08/31/1998	DAH WEN TSANG	1138-71	4972

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EXAMINER
LOKE, STEVEN HO YIN

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/144,579	Applicant(s) TSANG ET AL.	
	Examiner Steven Loke	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *43-66,98-103,106 and 107* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *43-66,98-103,106 and 107* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The amendment filed 12/4/01 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: The three new paragraphs inserted before line 4 of page 12 and the three new paragraphs inserted after line 28 of page 14.

Applicant is required to cancel the new matter in the reply to this Office Action.

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 12/4/01 have been disapproved because they introduce new matter into the drawings. 37 CFR 1.121(a)(6) states that no amendment may introduce new matter into the disclosure of an application. The original disclosure does not support the showing of figs. 6B and 6C.

3. Claims 44, 45, 46, 65, 66 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification never discloses the exact location of the insulating layer formed over the gate conductor as claimed in claim 44. Is the insulating layer formed on the top of the source conductor or in some other places?

The specification never discloses an upper metal layer over the insulating layer and contacting the gate conductor through a via in the insulating layer as claimed in claim 44. It is unclear where is the location of the via in the insulating layer.

The specification never discloses the exact location of the insulating layer formed over the gate conductor as claimed in claim 46. Is the insulating layer formed on the top of the source conductor or in some other places?

4. Claims 44-46, 60-66, 98, 99-103, 106 and 107 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification never discloses the conductor that contacts with the gate conductor is made of metal as claimed in claim 44.

The specification never discloses a portion of the upper metal layer over the insulating layer contacts the source conductor in electrical isolation from the gate conductor as claimed in claim 45.

The specification never discloses an insulating layer over the gate conductor and an upper metal layer over the insulating layer and contacting the vertically-extending source conductor through a via in the insulating layer as claimed in claim 46.

The specification never discloses the conductor that contacts the source conductor is made of metal as claimed in claim 46.

The specification discloses the gate metal layer comprises a refractory metal silicide (page 11, line 27 to page 12, line 1). The specification never discloses the gate metal layer comprises aluminum and the upper metal layer comprises aluminum as claimed in claim 65. OK

The specification never discloses the gate metal layer comprises aluminum and the insulating layer comprises at least one of the group consisting of nitride, glass and PSG as claimed in claim 66.

The specification never discloses the gate metal layer comprises aluminum as claimed in claims 60 and 64.

The specification never discloses the gate metal layer comprises a plateable metal as claimed in claims 61 and 63.

The specification never discloses a refractory metal silicide beneath the gate metal layer as claimed in claim 62.

The specification never discloses an insulating layer disposed over the gate structure and metallization over the insulating layer and contacting the gate structure through the insulating layer as claimed in claim 98.

The specification never discloses the metal of the conductive gate structure comprises a metal on a refractory metal-silicide as claimed in claim 99.

The specification never discloses the metal of the conductive gate structure comprises plateable metal as claimed in claim 100.

The specification never discloses the insulative layer is deposited at temperature less than 430 C degree as claimed in claim 101.

The specification never discloses the gate metal comprises aluminum as claimed in claim 102.

The specification never discloses the metallization over the insulating layer comprises aluminum as claimed in claim 103.

5. Claims 50-52, 99, 106 and 107 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 50, line 3, "at least one vertically-oriented sidewall spacers" is unclear whether it is being referred to one vertically-oriented sidewall spacer or more than one vertically-oriented sidewall spacers.

In claim 51, line 3, "one of said vertically-oriented sidewall spacer" is unclear whether it is being referred to "one of said vertically-oriented sidewall spacers".

In claim 99, line 2, "a metal" is unclear whether it is being referred to the metal of claim 98.

In claim 106, line 3, "said vertical orientation" has no antecedent basis.

In claim 107, lines 3-4, "said vertically-oriented channel structures" has no antecedent basis.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 43, 47, 48, 50, 51, 53, 57, 58, 61 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto.

In regards to claim 43, 50, 51, 53, 57, Sakamoto discloses a transistor in fig. 4(d). It comprises: a gate trench formed on a drain substrate [1,3]; p-type body region [11] and

vertical channel and source regions [11, 12] formed between the trenches; insulating layer [4, 9] formed adjacent to the gate electrode [8]; the vertically-insulative layers [4] being formed by a deposited film of uniform lateral thickness and the laterally-extending insulative layer [9] being separately formed of a deposited isolation material; a metal source electrode [15] formed on the regions [11, 12, 9].

Sakamoto differs from the claimed invention by not having a gate metal layer coextending over the doped polysilicon of a gate conductor.

Fig. 2(d) of Sakamoto shows a metal silicide (tungsten silicide) layer formed on the polysilicon gate conductor [8] in a vertical MOSFET.

Since both figs. 4(d) and 2(d) of Sakamoto teach a polysilicon gate electrode in a vertical MOSFET, it would have been obvious to have the metal silicide layer of fig. 2(d) of Sakamoto in fig. 4(d) of Sakamoto because it reduces the resistance of the gate electrode.

It would have been obvious to have the oxide layer as the gate insulating layer because it is a conventional gate insulating material.

In regards to claim 47, fig. 4(d) of Sakamoto differs from the claimed invention by not showing the first vertical layer portion has a lateral thickness less than a vertical height thereof.

Fig. 3 of Sakamoto shows the first vertical layer portion [11] has a lateral thickness less than a vertical height thereof.

Since both figs. 4(d) and 3 of Sakamoto teach a source electrode formed in a trench in a vertical MOSFET, it would have been obvious to have the p-type base region of fig.

3 of Sakamoto in fig. 4(d) of Sakamoto because it reduces the resistance of the base region.

In regards to claim 48, it would have been obvious for the first vertical layer portion has a lateral thickness less than 1 micron because it depends on the size of the transistor cell and the packing density of the transistor cells.

In regards to claim 58, fig. 4(d) of Sakamoto differs from the claimed invention by not showing a base region made of p-type layer.

Fig. 7 of Sakamoto shows a p-type layer [1'] formed under the n-type layer [2, 3].

Since figs. 4(d) and 7 of Sakamoto show a vertical transistor, it would have been obvious to have the p-type layer of fig. 7 of Sakamoto in fig. 4(d) of Sakamoto because it can form a pnpn type transistor.

In regards to claims 61, 63, it would have been obvious for the gate metal layer comprises plateable metal since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

8. Claims 44-46, 52, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Bulucea et al.

In regards to claim 44, Sakamoto differs from the claimed invention by not showing an insulating layer over the gate conductor and an upper metal layer over the insulating layer and contacting the gate conductor through a via in the insulating layer.

Bulucea et al. shows an insulating layer [41] over the gate conductor [36a, 36b] and an upper metal layer [43a] over the insulating layer and contacting the gate conductor through a via in the insulating layer in figs. 21-31B.

Since both Sakamoto and Bulucea et al. teach a vertical MOSFET with a trench-type gate electrode, it would have been obvious to have the gate contact structure of Bulucea et al. in Sakamoto because it provides external connection between the MOSFET and the external circuit.

In regards to claim 45, the combined device shows a portion of the metal layer [43b of Bulucea et al.] over the insulating layer [41] contacts the source conductor in electrical isolation from the gate conductor.

In regards to claim 46, the combined device shows the insulating layer [9 of Sakamoto] over the gate conductor [8] and an upper metal layer [15] over the insulating layer and contacting the vertically-extending source conductor through a via in the insulating layer [9].

In regards to claim 52, the combined device shows an upper metal layer [15] extending over the insulative layer [9] and the vertically-oriented sidewall spacers and contacting the vertically-extending source conductor.

In regards to claim 55, the combined device shows the trench-type gate structure enclosing a plurality of cells that comprises the source conductor and the source and channel regions.

In regards to claim 56, the combined device shows the source conductor intermediate the plurality of gate fingers to define an interdigitated source-gate structure.

9. Claims 60, 62, 64, 65 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Bulucea et al., further in view of Temple.

In regards to claim 60, Sakamoto differs from the claimed invention by not showing the gate metal layer comprises aluminum.

Temple shows the gate metal layer [110] comprises aluminum in fig. 18.

Since both Sakamoto and Temple teach a gate electrode made of polysilicon and metal silicide, it would have been obvious to have the aluminum of Temple in Sakamoto because it reduces the contact resistance of the gate electrode.

In regards to claim 62, the combined device shows the gate conductor comprises a refractory metal silicide over the doped polysilicon, and beneath the gate metal layer.

In regards to claim 64, the combined device shows the gate metal layer comprises aluminum.

In regards to claim 65, the combined device shows the gate metal layer comprises aluminum, and the upper metal layer ([43a] of Bulucea et al.) comprises aluminum.

In regards to claim 66, the combined device shows the gate metal layer comprises aluminum, and the insulating layer ([41] of Bulucea et al.) comprises a glass (BPSG).

10. Claims 49 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Davies.

Sakamoto differs from the claimed invention by not showing a p+ type body region.

Davies shows a p+ type body region [21] formed in a p-type base region [17] in a vertical MOSFET in fig. 1.

Since both Sakamoto and Davies teach a vertical MOSFET, it would have been obvious to have the p+ type body region of Davies in Sakamoto because it prevents parasitic bipolar transistor turn on and it extends the safe operating area of the transistor.

11. Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Blanchard.

In regards to claim 59, Sakamoto further differs from the claimed invention by not showing a trench gate oxide with two different thickness.

Blanchard shows the gate oxide layer [32] having a thick oxide layer at the bottom of the gate trench and a thin oxide layer at the upper portion of the gate trench in fig. 3.

Since both Sakamoto and Blanchard teach a vertical MOSFET with a trench gate, it would have been obvious to have the gate oxide layer of Blanchard in Sakamoto because it increases the breakdown voltage of the device.

12. Applicant's arguments filed 12/4/01 have been fully considered but they are not persuasive.

It is urged, in page 14 of the remarks, that the written description of U.S. Patent No. 4,895,810 and the newly added fig. 6B from U.S. Patent No. 4,895,810 show a gate metal layer coextending over the doped polysilicon. However, the gate electrode of U.S. Patent No. 4,895,810 is directed to a vertical MOSFET having a gate electrode formed on a planar surface of the substrate. It is different from the trench-type gate

electrode of the present invention. The written description and the new figure from U.S. Patent No. 4,895,810 do not support the claimed invention. However, the metal silicide of the present invention is considered as the gate metal layer that coextending over the doped polysilicon.

It is urged, in page 14 of the remarks, that the written description of U.S. Patent No. 5,262,336 and the newly added fig. 6C from U.S. Patent No. 5,262,336 show a portion of the upper metal layer over the insulative layer contacting the source conductor in electrical isolation from the gate conductor. However, U.S. Patent No. 5,262,336 is directed to a vertical MOSFET having a gate electrode formed on a planar surface of the substrate. It is different from the trench-type gate electrode of the present invention. Therefore, the written description and the new figure cannot applied to the present invention. The specification also never discloses the upper metal layer that comprises gate contact connected to the source conductor.

It is urged, in page 15 of the remarks, that U.S. Patent Nos. 4,895,810 and 5,262,336 teach the subject matters of claims 46 and 60-65. However, both patents disclose a device different from the present invention. The patents disclose a vertical MOSFET having a gate electrode formed on a planar surface of the substrate while the present invention discloses a trench-type gate electrode. Therefore, the devices of the patents cannot applied to the device of the present invention.

It is urged, in page 15 of the remarks, that the insulating materials of claim 66 is support by the device in U.S. Patent No. 5,262,336. However, the patent discloses a passivation layer formed on the edge of the device. It never discloses the insulating

layer formed on the gate electrode. In addition, the patent disclose a vertical MOSFET having a gate electrode formed on a planar surface of the substrate while the present invention discloses a trench-type gate electrode. Therefore, the device of the patent cannot applied to the device of the present invention.

It is urged, in page 19 of the remarks, that claim 98 is supported by U.S. patent no. 4,895,810. However, the last two paragraphs of claim 98 are not supported by the patent.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
May 17, 2002

Steven Loke
Primary Examiner
Steven Loke